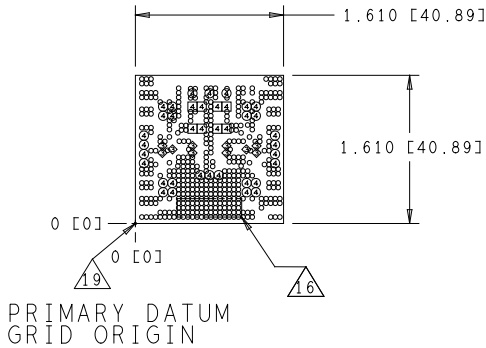


		2		1		
		REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED		
				DE	PE	CAD
	A	RELEASE TO PRODUCTION FROM 95992	20-04-26	D. U.	R. B.	A. C.

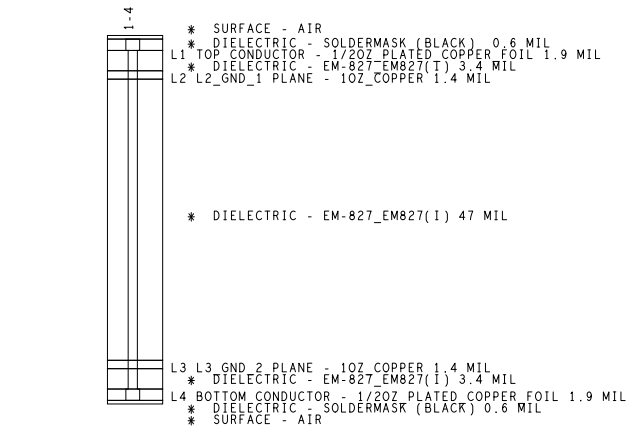
NOTES (UNLESS OTHERWISE SPECIFIED):

- THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.
 3. BASE MATERIAL - LAMINATE AND PREPREG SHALL BE PER INCLUDED STACKUP DATA.
T_g - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
T_d - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
 4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'
 5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'
 6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .0055"/.005"
 7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).
 8. FAB VENDOR IS NOT ALLOWED TO USE ODB FOR FABRICATION. CAN BE USED ONLY FOR REFERENCE.
 9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
TYPE: LPI OR EQUIVALENT.
A. LOCATION = +/- .002" OF PLATED PADS.
B. DIAMETER OR SIZE = +/- .002 OF ORIGINAL DATA
 10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.
 11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.
 12. PRINTED WIRING BOARDS TO BE SEPARATED BY FOIL OR AN EQUIVALENT METHOD IN THE PACKAGE.
 13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.
 14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.
 15. TWO SOLDER SAMPLES TO BE PROVIDED.
NOT ALLOWING MECHANICAL CONTACT BETWEEN THEM TO AVOID SCRATCHES.
 16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0
 17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)
 18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)
 19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.
 20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.
 21. THIEVING REQUIREMENT:
A. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS.
KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.
 22. THIS BOARD USES VIA-IN-PAD.
A. ALL VIAS IN PADS ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL AND MADE PLANAR TO THE PADS.
B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
C. DIMPLE ON VIA-IN-PADS MUST BE NO GREATER THAN .003" AND PROTRUSION NO GREATER THAN .002"
 23. WORKING GERBER CAN BE REQUESTED BY NXP CAD ENGINEER IN SPECIFIC PROJECTS DURING EOS.
CAD ENGINEER WILL PROVIDE APPROVAL FOR WORKING GERBER.



DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

LAYERS	SINGLE ENDED			DIFFERENTIAL		
	TRACE WIDTH (MILS)	IMPEDANCE (OHMS)	REFERENCE LAYER	TRACE WIDTH (MILS)	TRACE SPACING "AIR GAP" (MILS)	IMPEDANCE (OHMS)
L1_PS	5.50	50	L2	N/A	N/A	N/A
L4_SS	5.50	50	L3	N/A	N/A	N/A



DESIGN CROSS SECTION CHART
TOTAL THICKNESS 61.6 MIL
BOARD THICKNESS TOLERANCE +/-10%
ALL VALUES ARE FINISHED VALUES

DETAIL A
LAYER STACKUP
SCALE: NONE

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE ROHS COMMISSION DELEGATED DIRECTIVE (EU) 2015/863 AND THE COMMISSION AMENDING DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

-----	COMPANY PUBLIC
<u>X</u> -----	COMPANY INTERNAL
-----	COMPANY CONFIDENTIAL

UNLESS OTHERWISE SPECIFIED
 DIMENSIONS ARE IN INCHES
 TOLERANCES ARE:

DECIMALS	ANGLES
.XX .01	.0-30°
.XXX .005	

✓ FMS ALL MACHINED SURFACES
 BREAK ALL SHARP EDGES AND CORNERS.
 REMOVE BURRS.
 UNDERLINED DIM. NOT TO SCALE.
 THIRD ANGLE ORTHOGRAPHIC PROJECTION IS
 USED.

PART NO. 170-96736		NXP SEMICONDUCTORS 6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA				
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.						
APPROVALS		DATE	TITLE: PRINTED WIRING BOARD P3B1602DP-EVB			
DRAWN ALDO CARO		20-04-26				
CHECKED R. BOBADILLA		20-04-26	SIZE	CAD FILE NAME	DWG. NO.	REV
DESIGN ENGINEER DANIEL URIBE		20-04-26	☐ LAY-96736	FAB-96736		A
SCALE			1 / 1	DO NOT SCALE DRAWING		SHEET 1 OF 1